FIGURE 1

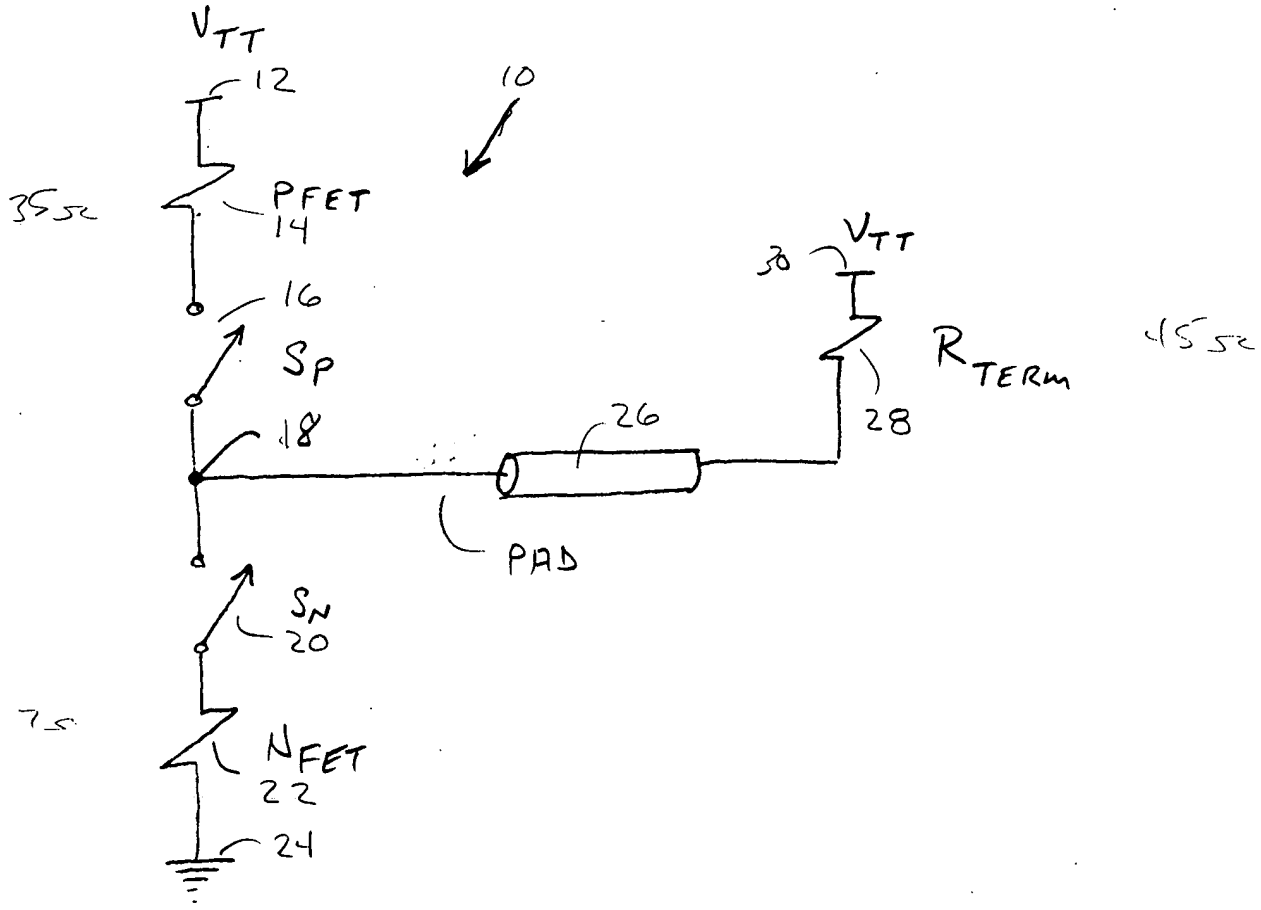
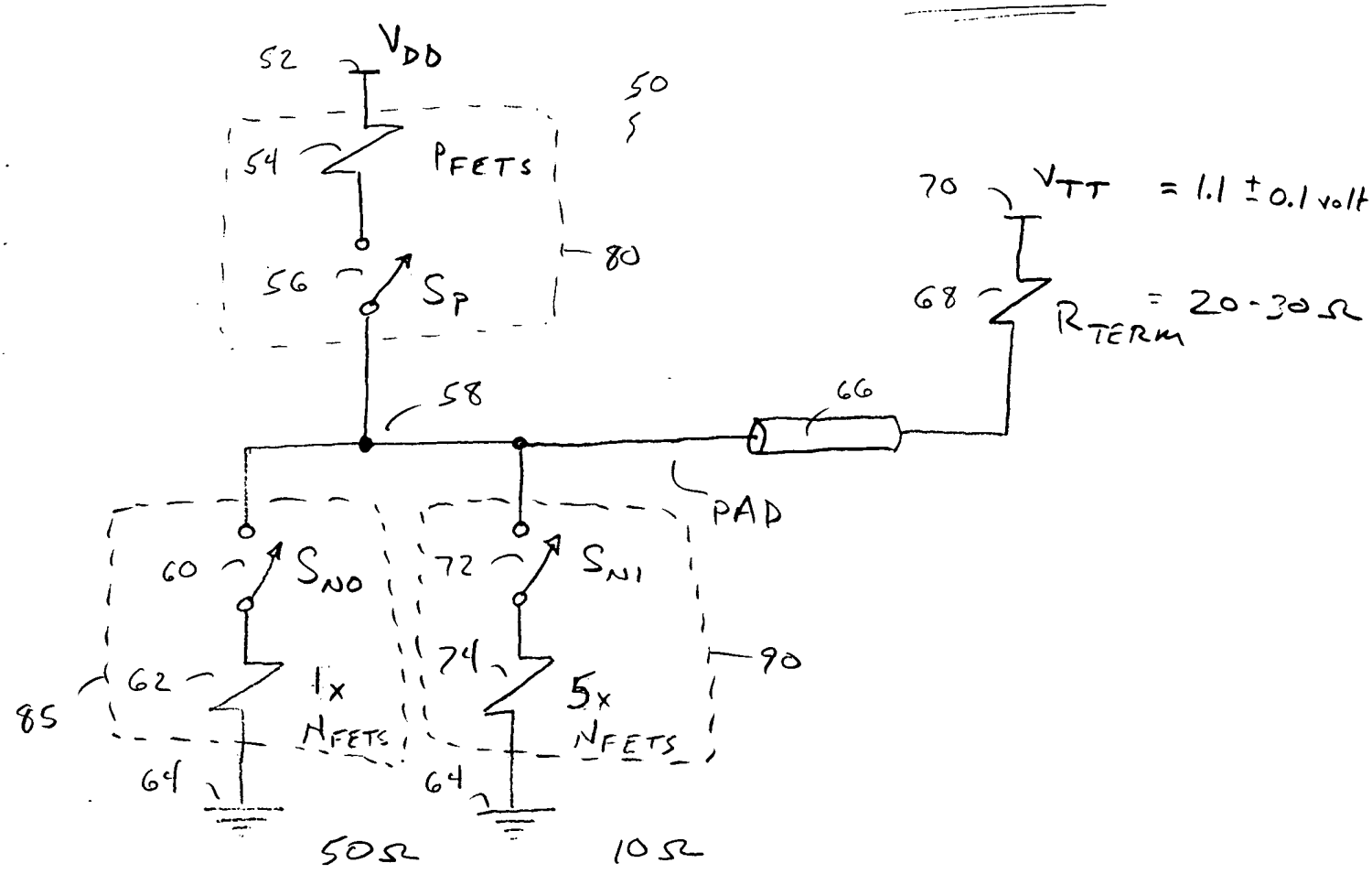

V_{TT}
12
10
35Ω
PFET
14
V_{TT}
30
16
S_P
R_{TERM}
45Ω
18
26
28
PAD
S_N
20
7Ω
NFET
22
24

FIGURE 2A


52
V_{DD}
50
54
PFETs
70
V_{TT} = 1.1 ± 0.1 volt
80
56
S_P
68
R_{TERM} = 20-30 Ω
58
66
PAD
60
S_{N0}
72
S_{N1}
90
62
1x
NFETs
74
5x
NFETs
85
64
64
50Ω
10Ω

080820 6290296

FIGURE 2B

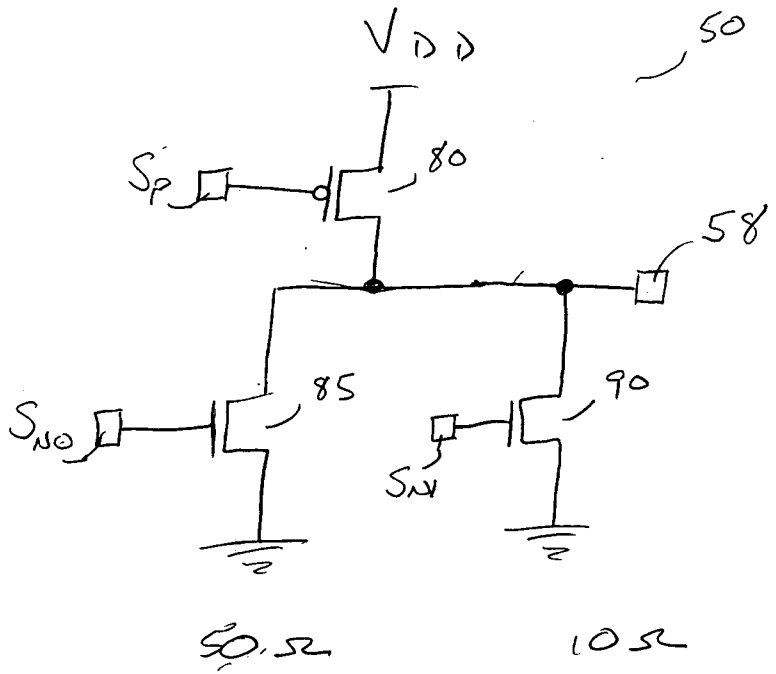
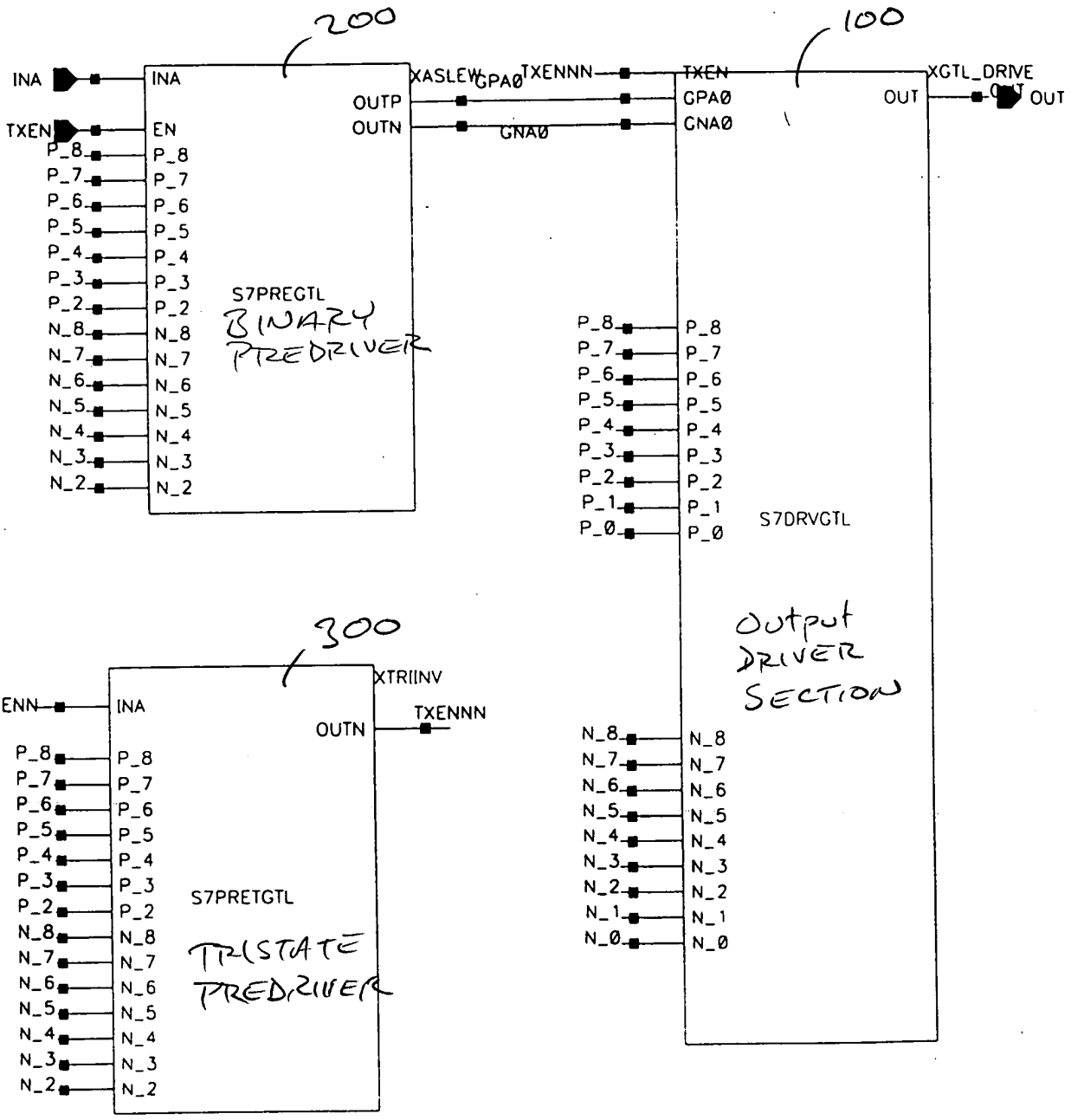


FIGURE 3


200
100
300
INA
TXEN
P_8
P_7
P_6
P_5
P_4
P_3
P_2
N_8
N_7
N_6
N_5
N_4
N_3
N_2
EN
OUTP
OUTN
XASLEW
GPA0
GNA0
TXENNN
S7PREGTL
BINARY PREDRIVER
TXEN
GPA0
GNA0
P_1
P_0
OUT
XGTL_DRIVE
S7DRVGTL
Output DRIVER SECTION
TXENN
XTRIINV
S7PRETGTL
TRISTATE PREDRIVER

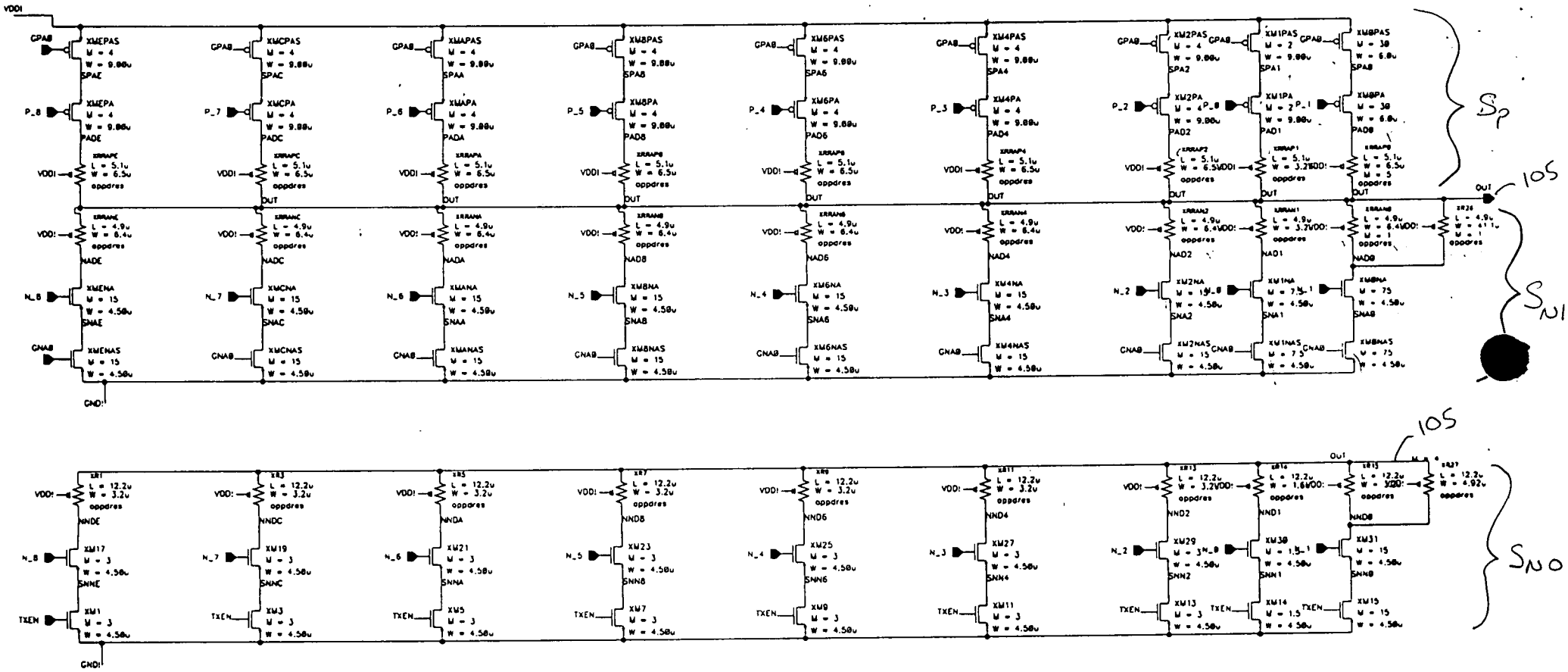

VDDI
GPAB
XMEPAS
XMEPA
XMEPAC
XMEPAS
XMEPA
XMEPAC
XMEPAS
XMEPA
XMEPAC
XMEPAS
XMEPA
XMEPAC
XMEPAS
XMEPA
XMEPAC
XMEPAS
XMEPA
XMEPAC
P_8
P_7
P_6
P_5
P_4
P_3
P_2
P_1
VDDI
OUT
XRRAPE
XRRAPC
XRRAPA
XRRAP8
XRRAP6
XRRAP4
XRRAP2
XRRAP1
XRRAP9
oppdres
NADE
NADC
NADA
NAD8
NAD6
NAD4
NAD2
NAD1
NAD9
N_8
N_7
N_6
N_5
N_4
N_3
N_2
N_1
XMENA
XMCNA
XMANA
XM8NA
XM6NA
XM4NA
XM2NA
XM1NA
XM9NA
SNAE
SNAC
SNAA
SNA8
SNA6
SNA4
SNA2
SNA1
SNA9
GNAB
XMENAS
XMCNAS
XMANAS
XM8NAS
XM6NAS
XM4NAS
XM2NAS
XM1NAS
XM9NAS
GND!
Sp
SN1
IOS
XR1
XR3
XR5
XR7
XR9
XR11
XR13
XR15
XR17
XR19
XR21
XR23
XR25
XR27
XR29
XR31
NNDE
NNDC
NNDA
NND8
NND6
NND4
NND2
NND1
NND9
SNNE
SNNC
SNNA
SNN8
SNN6
SNN4
SNN2
SNN1
SNN9
TXEN
XM1
XM3
XM5
XM7
XM9
XM11
XM13
XM14
XM15
SN0

FIGURE 4A

FIGURE 4B

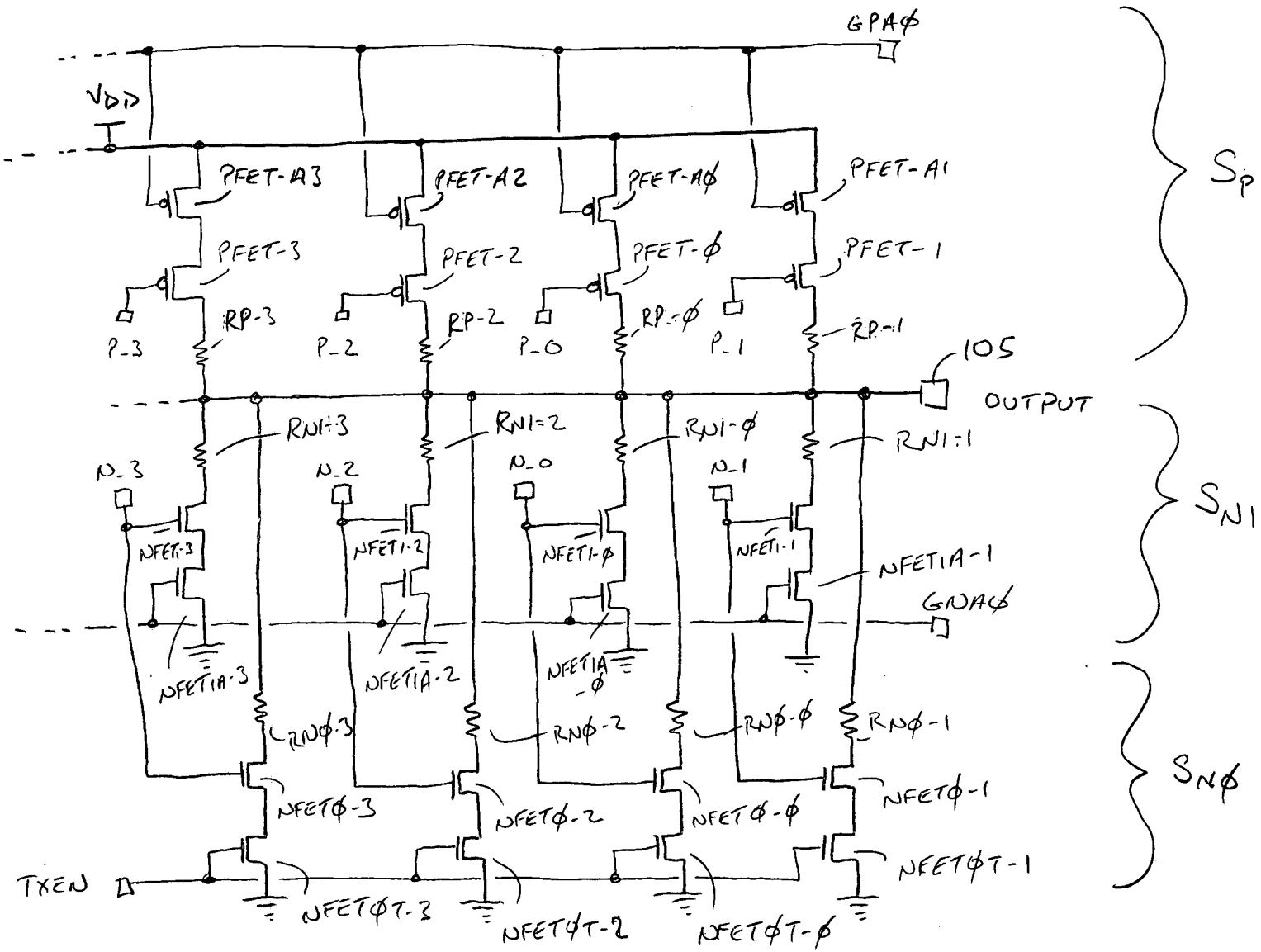
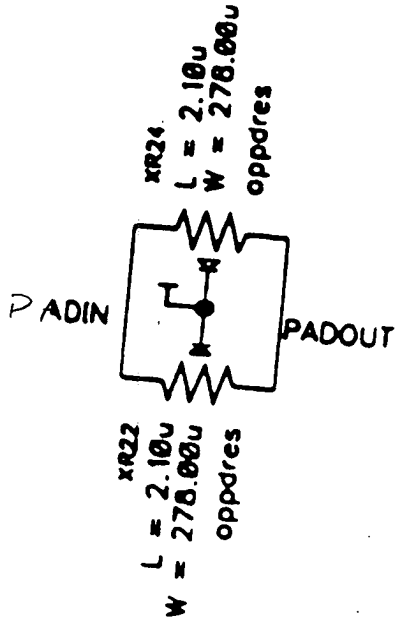

GPAφ
VDD
PFET-A3
PFET-A2
PFET-Aφ
PFET-A1
PFET-3
PFET-2
PFET-φ
PFET-1
RP-3
RP-2
RP-φ
RP-1
P_3
P_2
P_0
P_1
105
OUTPUT
RNI-3
RNI-2
RNI-φ
RNI-1
N_3
N_2
N_0
N_1
NFET-3
NFETI-2
NFETI-φ
NFETI-1
NFETIA-1
GNAφ
NFETIA-3
NFETIA-2
NFETIA-φ
RNφ-3
RNφ-2
RNφ-φ
RNφ-1
NFETφ-3
NFETφ-2
NFETφ-φ
NFETφ-1
TXEN
NFETφT-3
NFETφT-2
NFETφT-φ
NFETφT-1
SP
SNI
SNφ

FIGURE 5



SELECTABLE OP RESISTORS TO BE USE WITH PADXFER METAL (LM) TOTAL RESISTENT MATCHING UP TO 3 OHMS.

ONE RESISTORS L=2.1U AND W=93.0U = 3.0 OHMS
ONE RESISTORS L=2.1U AND W=111.0U = 2.5 OHMS
ONE RESISTORS L=2.1U AND W=139.0U = 2.0 OHMS
ONE RESISTORS L=2.1U AND W=185.0U = 1.5 OHMS
ONE RESISTORS L=2.1U AND W=278.0U = 1.0 OHMS
TWO RESISTORS L=2.1U AND W=278.0U IN PARALLEL = 0.5 OHMS SHOWN
ZERO RESISTORS TO BE USED FOR 0 OHMS

05208679.072101

FIGURE 6

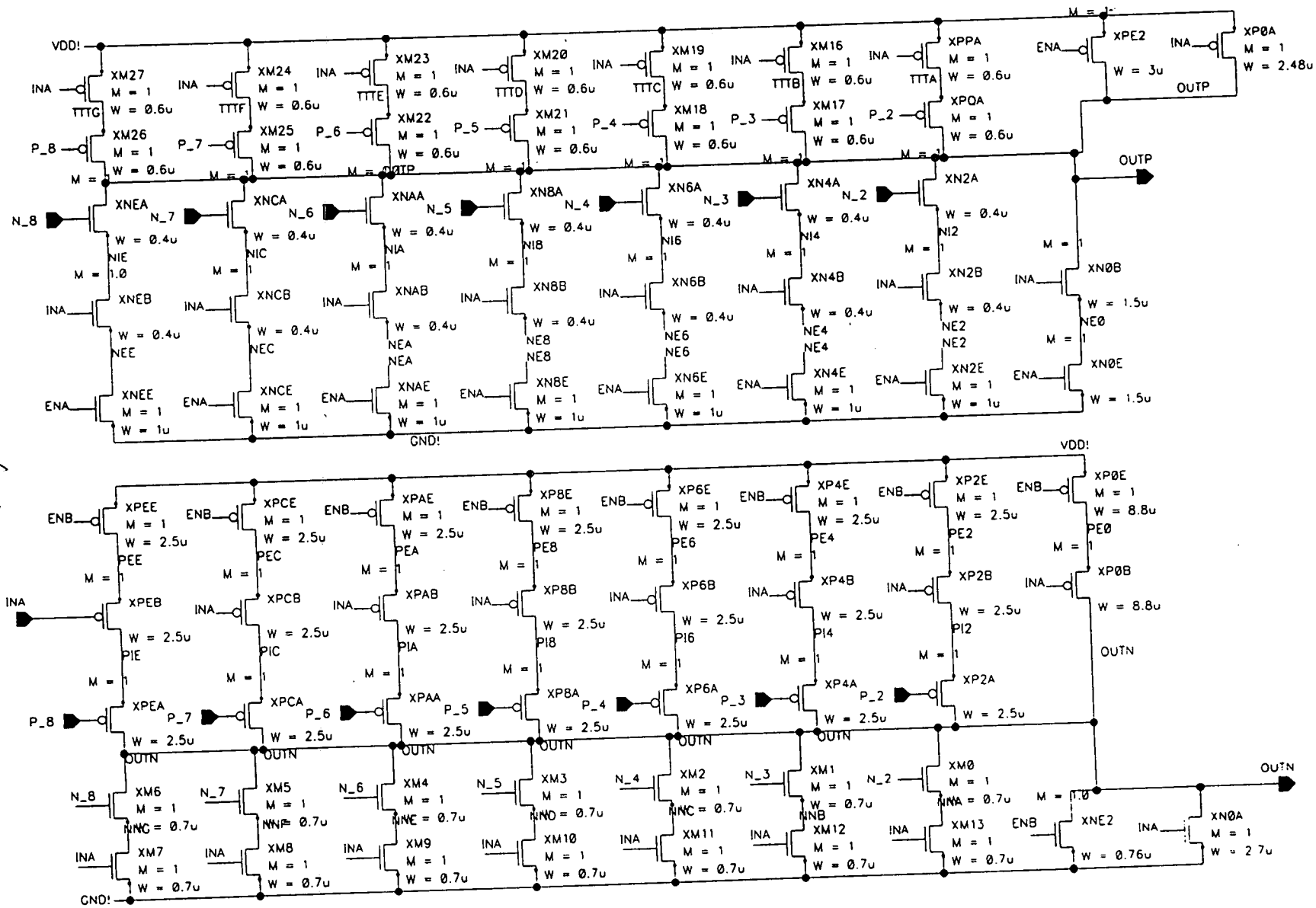
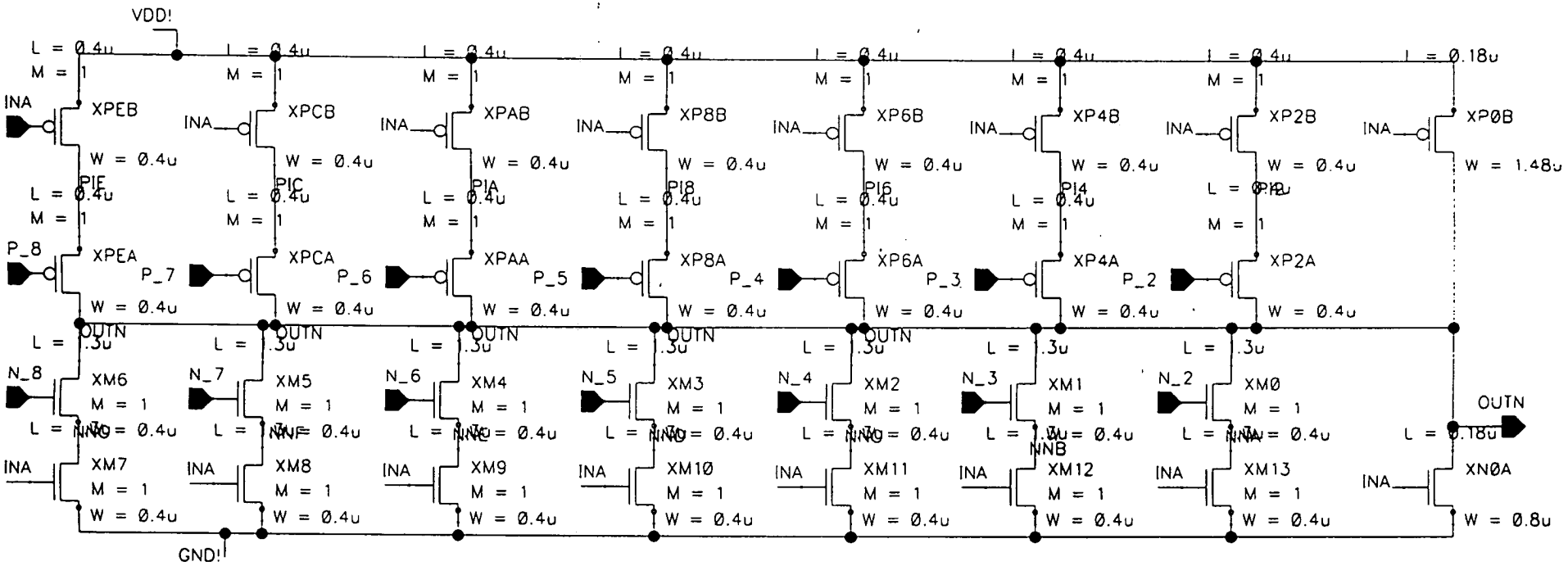

200
A
B
VDD!
GND!
INA
ENA
ENB
OUTP
OUTN
N_8
N_7
N_6
N_5
N_4
N_3
N_2
P_8
P_7
P_6
P_5
P_4
P_3
P_2
XM27
XM26
XM24
XM25
XM23
XM22
XM20
XM21
XM19
XM18
XM16
XM17
XPPA
XPQA
XPE2
XP0A
XNEA
XNEB
XNEE
XNCA
XNCB
XNCE
XNAA
XNAB
XNAE
XN8A
XN8B
XN8E
XN6A
XN6B
XN6E
XN4A
XN4B
XN4E
XN2A
XN2B
XN2E
XN0B
XN0E
XPEE
XPEB
XPEA
XPCE
XPCB
XPCA
XPAE
XPAB
XPAA
XP8E
XP8B
XP8A
XP6E
XP6B
XP6A
XP4E
XP4B
XP4A
XP2E
XP2B
XP2A
XP0E
XP0B
XM6
XM7
XM5
XM8
XM4
XM9
XM3
XM10
XM2
XM11
XM1
XM12
XM0
XM13
XNE2
XN0A

FIGURE 7

300


VDD!
GND!
INA
XPEB
XPCB
XPAB
XP8B
XP6B
XP4B
XP2B
XP0B
XPEA
XPCA
XPAA
XP8A
XP6A
XP4A
XP2A
XM6
XM5
XM4
XM3
XM2
XM1
XM0
XM7
XM8
XM9
XM10
XM11
XM12
XM13
XN0A
P_8
P_7
P_6
P_5
P_4
P_3
P_2
N_8
N_7
N_6
N_5
N_4
N_3
N_2
OUTN
NNB
L = 0.4u
M = 1
W = 0.4u
L = .3u
L = 0.18u
W = 1.48u
W = 0.8u

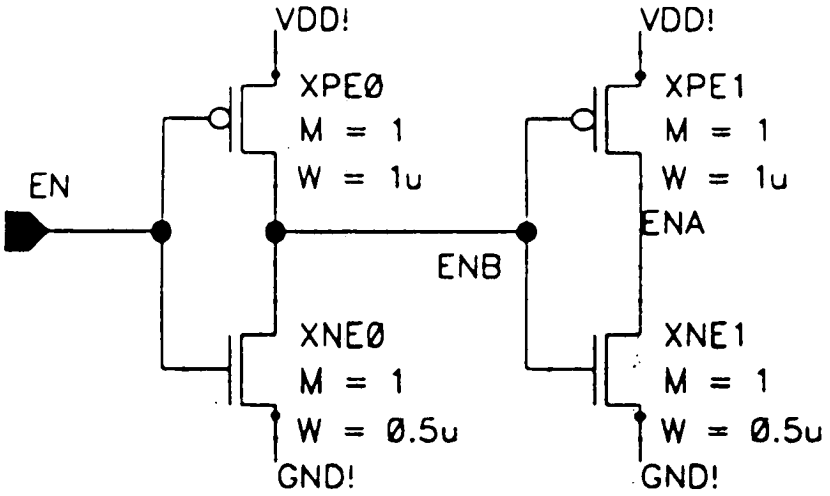

VDD!
XPE0
M = 1
W = 1u
EN
ENB
XNE0
M = 1
W = 0.5u
GND!
VDD!
XPE1
M = 1
W = 1u
ENA
XNE1
M = 1
W = 0.5u
GND!

FIGURE 8

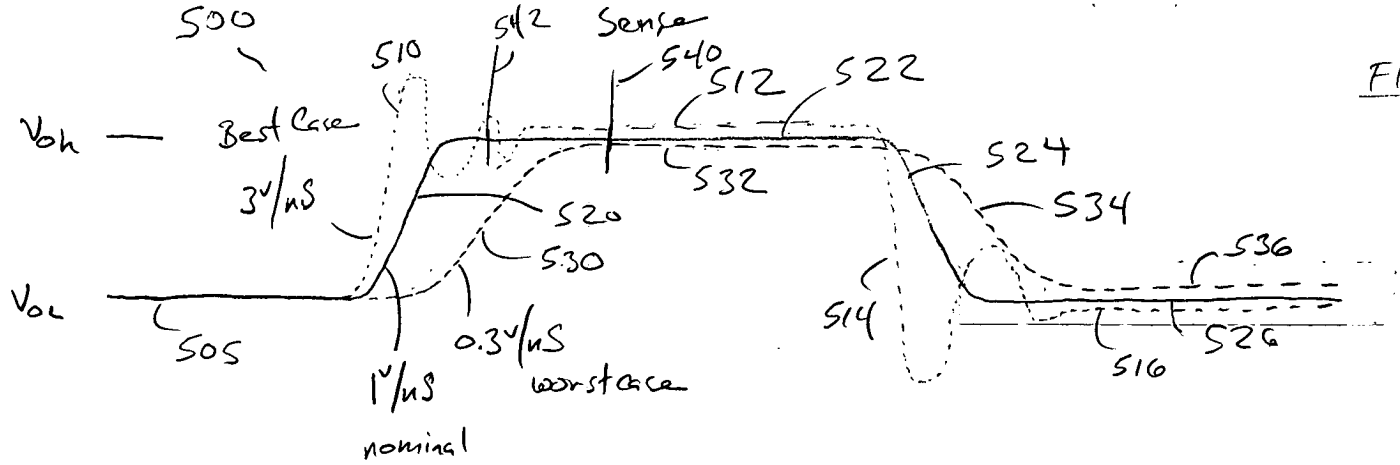


FIGURE 9A

Uncompensated

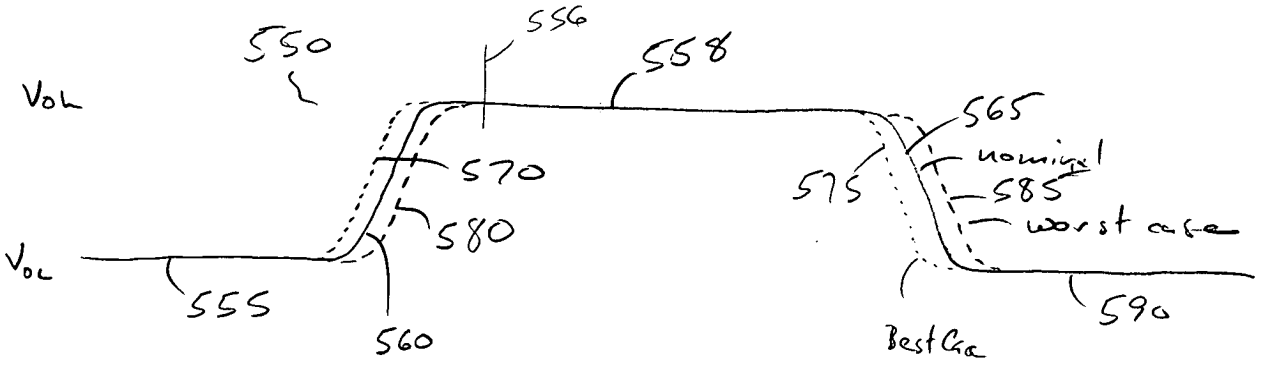


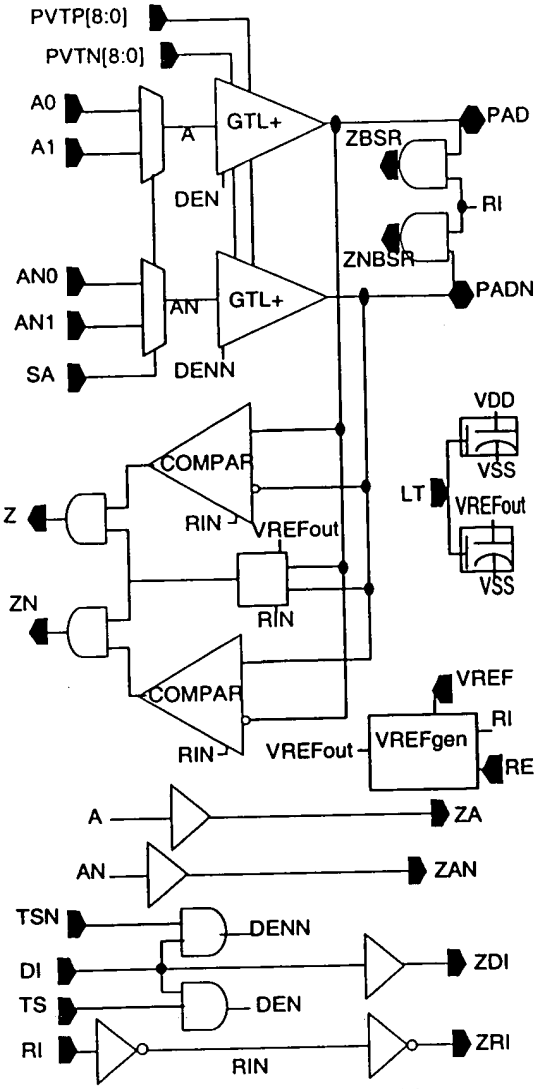
FIGURE 9B

Compensated

FIGURE 10

Description:
Non-inverting bidirectional driver/receiver that interfaces 1.8V internal functions with 1.1V enhanced GTL+ off-chip bidirectional data bus. The driver operates with a 1.8V supply. The driver has off-chip termination of 45 ohm to 1.1V (V_{TT}) at each end of the bus (double termination). The receiver has external reference V_{ref}(V_{TT}*2/3).

A0	Driver data0 input
A1	Driver data1 input
AN0	Driver data0 input
AN1	Driver data1 input
SA	Driver data select input
DI	Driver inhibit input (DI in)
TS	In-Phase Driver three-state control
TSN	Out-Phase Driver three-state control
PVTP[8:0]	PMOS edge rate control bus input
PVTN[8:0]	NMOS impedance control bus input
RE	Reference enable
RI	Receiver inhibit input (RI in)
VREF	(Vtt*2/3) input signal
PAD	In-Phase Driver output/receiver input
PADN	Out-Phase Driver output/receiver input
ZDI	Driver inhibit output (DI out)
ZRI	Receiver inhibit output (RI out)
Z	In-Phase Receiver output
ZN	Out-Phase Receiver output
ZA	Data0 test output (A0 or A1 out)
ZAN	DataN0 test output (AN0 or AN1 out)
ZBSR	PAD test output (PAD out)
ZNBSR	PADN test output (PADN out)
LT	Leakage test input



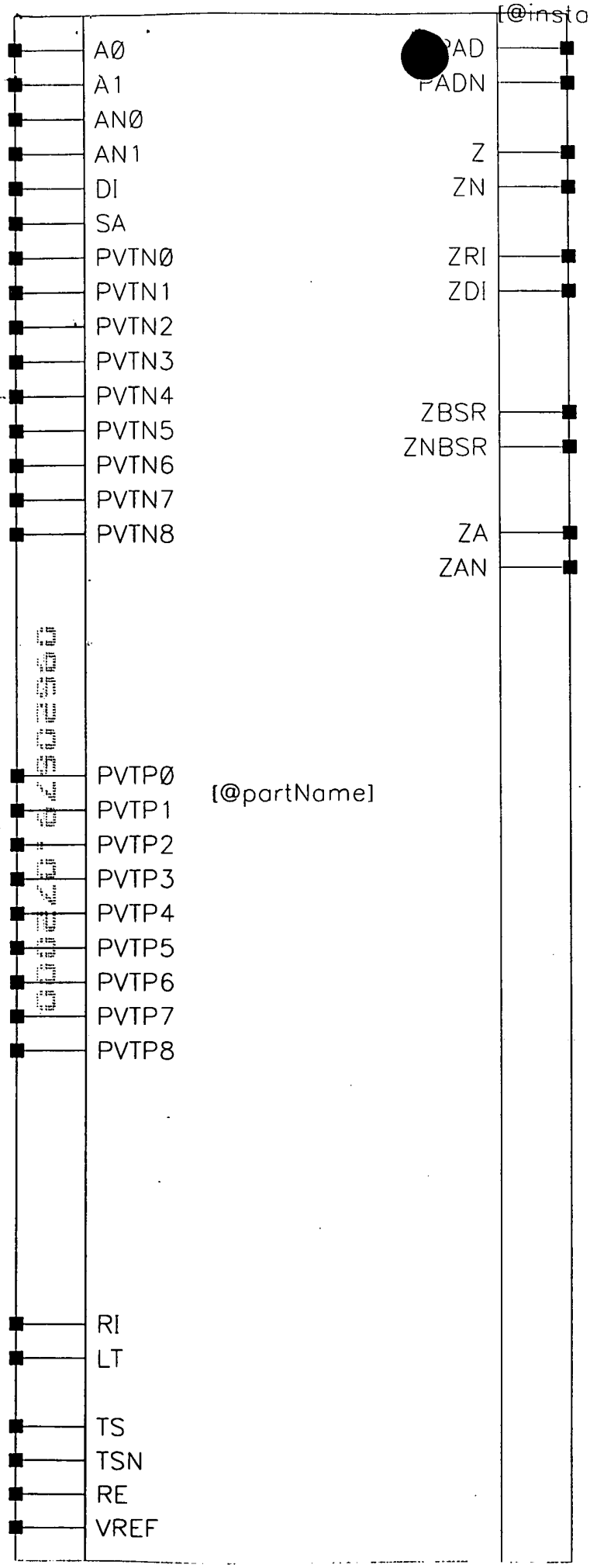

[@instanceName]
A0
A1
AN0
AN1
DI
SA
PVTN0
PVTN1
PVTN2
PVTN3
PVTN4
PVTN5
PVTN6
PVTN7
PVTN8
PAD
PADN
Z
ZN
ZRI
ZDI
ZBSR
ZNBSR
ZA
ZAN
PVTP0
PVTP1
PVTP2
PVTP3
PVTP4
PVTP5
PVTP6
PVTP7
PVTP8
[@partName]
RI
LT
TS
TSN
RE
VREF

FIGURE 11

FIGURE 12.

Driver Truth Table

Inputs							Outputs	
A0	A1	SA	TS	DI	PVTP	PVTN	PAD	Comments
-	-	-	0	-	-	-	Hi-Z[1]	High impedance mode
-	-	-	-	0	-	-	Hi-Z[1]	High impedance mode
-	-	-	-	-	0[2]	0[2]	Hi-Z[1]	PVT Test mode
0	-	0	-	-	-	0[2]	Hi-Z[1]	PVT Test mode
1	-	0	-	-	0[2]	-	Hi-Z[1]	PVT Test mode
0	-	0	1	1	-	>0	0[3]	PVT Test mode [3]
1	-	0	1	1	>0	-	1[3]	PVT Test mode [3]
0	-	0	1	1	>0	>0	0[3]	Functional, A0 data mode
0	-	0	1	1	1	1	0[3]	Functional, 10 Ohms @ BC
0	-	0	1	1	4	4	0[3]	Functional, 10 Ohms @ NOM
0	-	0	1	1	8	8	0[3]	Functional, 10 Ohms @ WC
1	-	0	1	1	>0	>0	1[3]	Functional, A0 data mode
-	-	1	1	1	>0	>0	A1	Functional, A1 data mode

1. PAD is at "V_{TT}" when connected to off-chip terminator.

2. When PVT= 0 all PVT bits go to vss and are off.

3. PAD Logical "1" = Vtt = 1.1V, Logical "0" = 0.4v or less

Notes: A. Vdd=1.8(+/- 0.1)V, Vtt = 1.1(+/- 0.02)V

B. During module external I/O test and system mode, driver output pullup is made by the external 22.5 ohm resistor to Vtt.

C. NDR will be based on driver terminated off-chip.

D. A0, A1, AN0, and AN1 are independent from each other

E. Entries in columns PVTP, PVTN represent number of lines held at logic "1" state. For testing the Impedence Controller forces PVTP and PVTN to 4 (i.e. PVTP[8:0]=PVTN[8:0]=[000011110] for all supply voltage levels.

FIGURE 13

Driver Truth Table

Inputs							Outputs	
AN0	AN1	SA	TSN	DI	PVTP	PVTN	PADN	Comments
-	-	-	0	-	-	-	Hi-Z[1]	High impedance mode
-	-	-	-	0	-	-	Hi-Z[1]	High impedance mode
-	-	-	-	-	0[2]	0[2]	Hi-Z[1]	PVT Test mode
0	-	0	-	-	-	0[2]	Hi-Z[1]	PVT Test mode
1	-	0	-	-	0[2]	-	Hi-Z[1]	PVT Test mode
0	-	0	1	1	-	>0	0[3]	PVT Test mode [3]
1	-	0	1	1	>0	-	1[3]	PVT Test mode [3]
0	-	0	1	1	>0	>0	0[3]	Functional, A0 data mode
0	-	0	1	1	1	1	0[3]	Functional, 10 Ohms @ BC
0	-	0	1	1	4	4	0[3]	Functional, 10 Ohms @ NOM
0	-	0	1	1	8	8	0[3]	Functional, 10 Ohms @ WC
1	-	0	1	1	>0	>0	1[3]	Functional, A0 data mode
-	-	1	1	1	>0	>0	A1	Functional, A1 data mode

1. PAD is at "V_{TT}" when connected to off-chip terminator.
2. When PVT= 0 all PVT bits go to vss and are off.
3. PAD Logical "1" = Vtt = 1.1V, Logical "0" = 0.4v or less
Notes: A. Vdd=1.8(+/- 0.1)V, Vtt = 1.1(+/- 0.02)V
B. During module external I/O test and system mode, driver output pullup is made by the external 22.5 ohm resistor to Vtt.
C. NDR will be based on driver terminated off-chip.
D. A0, A1, AN0, and AN1 are independent from each other
E. Entries in columns PVTP, PVTN represent number of lines held at logic "1" state. For testing the Impedence Controller forces PVTP and PVTN to 4 (i.e. PVTP[8:0]=PVTN[8:0]=[000011110] for all supply voltage levels.

FIGURE 14

Driver Propagation Delays (no load on outputs).

Path (Input to Output)	Performance Level	Parameter	Delay (ns) = intercept + slope (D_{std})[1]		
			V_{dd} = 1.7[2]V V_{tt} = 1.08V T_j = 100°C Process = Slow	V_{dd} = 1.8V V_{tt} = 1.1[3]V T_j = 60°C Process = Nom.	V_{dd} = 1.9[2]V V_{tt} = 1.12V T_j = 25°C Process = Fast
A0-PAD	A	t_{PLH}	1.2 ns	1.0 ns	0.8 ns
		t_{PHL}	1.2 ns	1.0 ns	0.8 ns
AN0-PADN	A	t_{PLH}	1.2 ns	1.0 ns	0.8 ns
		t_{PHL}	1.2 ns	1.0 ns	0.8 ns

1. *D_{std} is the number of standard loads.*
2. *Voltage at the package pin.*
3. *Design is optimized for Vtt=1.1v can be used for Vtt=1.0v to 1.2v.*

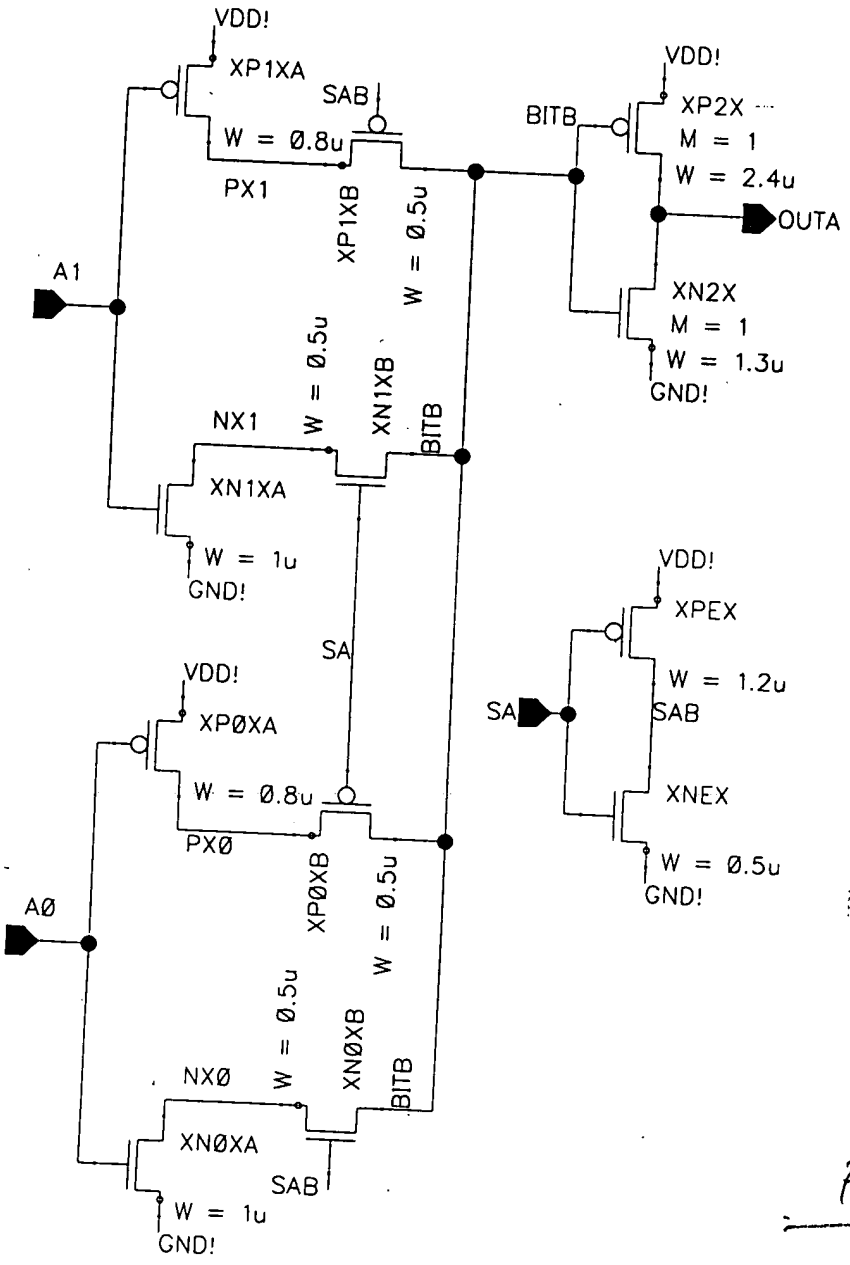

VDD!
XP1XA
SAB
W = 0.8u
PX1
XP1XB
W = 0.5u
A1
W = 0.5u
XN1XB
BITB
NX1
XN1XA
W = 1u
GND!
VDD!
XP2X
M = 1
W = 2.4u
OUTA
BITB
XN2X
M = 1
W = 1.3u
GND!
SA
VDD!
XPEX
W = 1.2u
SAB
SA
XNEX
W = 0.5u
GND!
VDD!
XP0XA
W = 0.8u
PX0
XP0XB
W = 0.5u
A0
W = 0.5u
XN0XB
BITB
NX0
XN0XA
SAB
W = 1u
GND!

FIGURE 15